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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,324	01/05/2004	Raminda Udaya Madurawe		1991

33380 7590 08/24/2006

RAMINDA U. MADURAWE
882 LOUISE DRIVE
SUNNYVALE, CA 94087

EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/751,324	MADURAWE, RAMINDA UDAYA
	Examiner	Art Unit
	Daniel D. Chang	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed August 3, 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 7,038,490 B1, hereinafter "Singh") in view of Duong et al. (US 5,600,264, hereinafter "Duong").

Regarding claim 1, Singh discloses an integrated circuit (IC) (col. 1, lines 6+) comprising:

a first selectable fabrication option (FPGA 5 in Fig. 1 and circuit shown in Fig. 5) comprised of a user configurable circuit (multiplexer 505; col. 4, lines 50+): and

a second selectable fabrication option (ASIC in Fig. 2 and circuit shown in Fig. 6) comprised of a hard-wired circuit in lieu of said user configurable circuit (col. 5, lines 3-57), wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options (col. 5, lines 3-57).

Singh does not explicitly teach that the configurable circuit is a configurable memory circuit and Singh is silent about the inherent select signals connected to the multiplexer 505.

However, Duong teaches that the select signals of the configurable circuit (multiplexer 110) is coupled to configurable memory circuit 232 and 234. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the user configurable circuit (multiplexer 505) of Singh with the configurable memory circuit 232 and 234 as taught by Duong in order to provide configurable signal to control and program the multiplexer 505.

Regarding claim 2, Singh in view of Duong discloses, in Figs. 2-5 of Duong, that wherein said first selectable option comprises a configurable Random Access Memory (RAM) module (SRAM; col. 4, lines 48+).

Regarding claim 3, Singh in view of Duong discloses that wherein said second selectable option comprises a Read Only Memory (ROM) module (610 of Singh can be broadly interpreted as ROM).

Regarding claim 4, Singh in view of Duong discloses an input (X6, X2, X1, F/Q in Fig. 5 of Singh), said input received at an input-pad (inherent input pad in IC; see col. 1, lines 6+); and an output (590), said output generated at an output-pad (inherent output pad in IC; see col. 1, lines 6+); and an input to output signal propagation delay (col. 4, lines 65+), said delay substantially identical (col. 5, lines 3+) between said first and said second selectable fabrication options.

Regarding claim 5, Singh in view of Duong discloses that wherein said hard-wire circuit comprises at least one custom mask (see Fig. 6 in Singh), said at least one mask facilitating:

a power-bus (VCC in Figs. 3-4b) connection to replace a logic one in said configurable memory circuit; and a ground-bus (VSS in Figs. 3-4b) connection to replace a logic zero in said configurable memory circuit.

Regarding claim 6, Singh in view of Duong discloses that wherein said RAM element is selected from one of volatile and non-volatile memory elements (see col. 4, lines 48+ in Duong).

Regarding claim 7, Singh in view of Duong discloses that wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements (see col. 4, lines 48+ in Duong).

Claims 8-13 and 16 are essentially the same as claims 1-7 as discussed above and are rejected similarly.

Regarding claim 14, Singh in view of Duong discloses a pass-gate logic element (multiplexer 505 or 580 in Fig. 5 of Singh), said logic element providing a programmable means (memory 232 and 234 in Duong) for electrically connecting or disconnecting two nodes (any one of 20 inputs and output of multiplexer 505 or 580).

Regarding claim 15, Singh in view of Duong discloses that wherein said programmable means in said first selectable option comprises configuring a RAM bit (232, 234 of Duong), said RAM bit generating: a logic one output to connect said two nodes; and a logic zero output to disconnect said two nodes (Low and High state of select signals of multiplexer 505 or 580 in Fig. 5 of Singh).

Claims 17-20 are essentially the same as claims 1-16 as discussed above and are rejected similarly.

Response to Arguments

Applicant's arguments, filed August 3, 2006, with respect to last Office Action have been fully considered and the finality of that action has been withdrawn.

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel D. Chang
Primary Examiner
Art Unit 2819

DANIEL CHANG
PRIMARY EXAMINER

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